S E. | B1CMED | Sem-IV | (R) | LC | DEC-20 ||

V-2nd-HF-EX-11-D-11

Con. 6786-11. **MP-4366**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions from the remaining **six** questions.
(3) Assume **suitable** data wherever **necessary.**

1. (a) Convert $(782{\cdot}56)_{10}$ to :— 4
(i) BCD (ii) Hexadecimal (iii) Octal (iv) Binary.

(b) Do the following arithmetic operation :— 4
(i) $(742{\cdot}23)_8 + (32{\cdot}15)_8$
(ii) $(7\ AD{\cdot}5\ C)_{16} - (15\ D{\cdot}2\ A)_{16}$ use 16's complement
(iii) $(523{\cdot}6)_{BCD} + (728{\cdot}9)_{BCD}$
(iv) $(11001{\cdot}101)_2 - (1011{\cdot}01)_2$ use 1's complement

(c) Derive characteristic equation of JK Flip Flop. 4

(d) State and prove De Morgan's theorem. 4

(e) Explain how two half subtractors can be connected to form full subtractor. 4

2. (a) Reduce the following using KMap and implement using NAND gates. 10
(i) $f(A, B, C, D) = A\overline{B} + AB\overline{C}D + C\overline{D} + B$
(ii) $y(A, B, C, D) = \pi M(0, 2, 4, 5, 8, 9, 10, 12)$

(b) Implement the expression :— 10

$$y = A\overline{B} + CD + AB\overline{C} + B\overline{C}D$$

using (i) Single 8 : 1 MUX and gates.
(ii) 4 line to 16 line decoder and gates.

3. (a) What is the difference between synchronous and asynchronous counters ? 10
Design a three bit up-down synchronouos counter using JK Flip Flop.

(b) Reduce the following Boolean expression using Boolean laws and implement using NAND gates. 10

(i) $y = \overline{A}\left(A + \overline{B}\right)\left(A + \overline{C}\right)\left(\overline{A} + B\right) + \overline{C}\left(C + \overline{A}\,\overline{B}\right)$

(ii) $y = \overline{\left(\overline{\overline{A\,\overline{B}} + \overline{C}}\right) + \overline{A + B}}$

(iii) $y = \overline{\overline{A}\,B\,C} + \left(\overline{\overline{B} + \overline{C}}\right)\overline{A}$

(iv) $\overline{A \cdot \overline{B} \cdot C + B\,C}$

4. (a) What is race around condition in JK Flip flop ? Explain Master Slave JK Flip Flop and show the problem of race around condition avoided in MS-JK Flip Flop. 10

(b) Compare TTL and CMOS logic families. Draw the TTL NAND gate and explain the totem pole output. 10

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5. (a) Design a 2 bit comparator using gates. Show the truth table. K Map and steps for Design. 10

   (b) Explain the different types of shift registers. Using serial in serial out shift register draw a ring counter. 10

6. (a) Design a BCD to seven segment decoder for common Cathode type of display. Use gates for design. 10

   (b) Reduce the following function using Quine Mc Clusky Algorithm. 10

   $f(A, B, C, D) = \Sigma m (0, 1, 2, 5, 6, 7, 8, 9, 10, 12, 15)$

7. (a) Explain the rules for BCD addition. Design a BCD adder using IC 7483 and gates. 10

   (b) Explain any two :— 10

   (i) ALU

   (ii) Hamming Code

   (iii) Diode ROM.

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