Q1 a) Differentiate sequential dataflow, structural & behavioural modelling styles in
b) Explain surface inversion condition in MOS structure with help of band diag
c) Explain Latch up in CMOS.
d) Design NMOS ckt $F = \bar{X}YZ + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}$ and also draw stick diagram.

Q2)
a) Explain FPGA architecture. Also explain the config logic block (CLD) & I/P, O/P block of XC400 (15)
b) VHDL code for 2:4 decoder using process statement. (5)

Q3)
a) Differentiate const vol & const field scaling (10)
b) Consider CMOS system with following parameter, $\sigma_{ox} = q \times 2 \times 10^{10}$ /cm^2, $\epsilon_{ox} = 3.97\,\epsilon_0$ $t_{ox} = 200\,A^\circ$, $\phi_{GC} = -0.85$, $N_A = 2 \times 10^{15}$ /cm^3 $\epsilon_{si} = 11.7\,\epsilon_0$, $T = 300^\circ K$, $\epsilon_0 = 8.85 \times 10^{-14}$. Determine V_{TO} under zero bias at R.T.

Q4)
a) Explain photolithography.
b) Explain following semiconductor manfacturing process
(i) Oxidation (ii) Diffusion (iii) Ion implantation.

Q5
a) Write a VHDL code for 4 bit up-down counter.
b) Explain the terms noise immunity & noise margin w.r.t CMOS circuit.

Q6
a) Design CMOS ckt $Z = \overline{A(D+E) + BC}$
b) Draw voltage transfer ckts of following inverter:
(i) Resistive load Inverter.
(ii) Inverter with E-nMOS as pull-up
(iii) Inverter with D-nMOS as pull-up.
(iv) CMOS invertor.

Q7
(a) Draw ckt diag stick & layout of 2i/p NOR using CMOS (15)
(b) Explain hot-electron effect.