N.B. : (1) Question No. 1 is compulsory.
(2) Attempt any four from the remaining questions.
(3) Assume data if necessary, clearly mention it.
(4) Layout should be drawn on graph sheet. Use colour pencil for stick diagram.

1. (a) Explain different types of Modelling in VHDL Languages. 5
(b) Draw circuit diagram and stick diagram for the following function $y = a + ab$. 5
(c) What is the function of photo resist material in VLSI fabrication. Compare different types of photo resist materials 5
(d) Explain "Hot electron" effect. 5

2. (a) Explain data types in VHDL. 7
(b) Explain Features of VHDL. 3
(c) Write code for 4-bit up counter process statement. 10

3. (a) Explain architecture of CPLD XC–9500. 10
(b) Write VHDL code for 4:1 HUX. 5
(c) Write VHDL code for 1 bit full adder. 5

4. (a) Explain structure and operation of MOS transistor in linear and saturation region also draw band diagram of MOS structure at surface inversion 10
(b) Explain the circuit operation of CMOS inverter in the following cases :– 10
(i) when $V_{in} < V_{TO, n}$ (ii) $V_{in} = V_{iL}$
(iii) $V_{in} = V_{TH}$ (iv) $V_{in} = V_{iH}$
(v) $V_{in} > (V_{DD} + V_{TO,P})$.

5. (a) Compare MOS inverter with (i) Passive load (ii) E-nMOS as pull up (iii) D-nMOS as pull up (iv) CMOS inverter. 10
(b) Draw the circuit diagram, stick diagram and layout of 2-input NAND gate. 10

6. (a) Explain twin tub fabrication process in detail. 10
(b) Compare constant voltage and field scaling. 10

7. (a) Design $y = \bar{x}a + xb$ using complementry MOSFET. 8
(b) Calculate the threshold votage V_{TO} at $V_{SB} = 0$, for a polysilicon gate n-channel MOS transistor, with the following parameters substrate doping density $N_A = 10^{16}$ cm^{-3}. Polysilicon gate doping density – $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness = 500 A° and oxide-interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2} 12