(3 Hours) [Total Marks : 100

N.B. (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Draw **neat** labelled **diagrams** wherever **necessary**.
(4) Assumptions should be **clearly** stated.

1. (a) What is Scaling ? State advantages and disadvantages of scaling. 20
   (b) State the features of VHDL.
   (c) Explain Latch up in CMOS.
   (d) Implement the following function using CMOS technology :—
   $F_1 = \overline{XYZ + XW}$

2. (a) Explain the FPGA architecture. Also explain the Configurable Logic Block (CLB) and Input Output Block (IOB) of XC400. 10
   (b) Explain advantages and disadvantages of ion implantation over diffusion. 10

3. (a) Write VHDL Code for 4 bit full adder. 10
   (b) Explain Photolithography in detail. 10

4. (a) Derive Noise Margin parameters (NMH and NML) for resistive load MNOS inverter. 10
   (b) Differentiate between PMOS and NMOS. 10

5. (a) Consider CMOS system with following parameters :— 10
   (i) $t_{OX} = 200$ A°
   (ii) $\phi_{GC} = -0.85$
   (iii) $N_A = 2 \times 10^{15}/cm^3$
   (iv) $Q_{OX} = q \times 2 \times 10^{11} c/cm^2$
   (v) $\varepsilon_{OX} = 3.33\ \varepsilon_0$
   (vi) $\varepsilon_{si} = 11.4\ \varepsilon_0$
   (vii) $T = 300°K$
   (viii) $\varepsilon_0 = 8.85 \times 10^{-14}$
   Determine threshold voltage V_{to} under zero bias at room temperature.
   (b) Explain MOSFET capacitance in detail. 10

6. (a) Draw the stick diagram and layout of 2–i/p NAND gate using CMOS. 10
   (b) Draw voltage transfer characteristics of the following :— 10
   (i) Resistive Load Inverter
   (ii) Inverter with E – nMOS as pull up
   (iii) CMOS Inverter.

7. Write short notes on the following :— 20
   (a) Channel Length Modulation
   (b) Hot electron effect
   (c) Design rules and layout for CMOS
   (d) Thermal oxidation.