VT-F.H.Exam. April(1)-13-172

Con. 8215-13. **GS-3217**

(REVISED COURSE)

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. 1 is **compulsory**.
(2) Attempt any **four** questions from remaining **six** questions.
(3) Draw **neat** labelled diagrams wherever **necessary**.
(3) Assumptions should be **clearly** stated.

1. (a) What are the major capabilities that the VHDL language provides along with the features, that differentiate it from other hardware description languages. 5
(b) Write a VHDL code for 2:4 decoder using structural stye of modelling. 5
(c) What are the limitations of PMOS and NMOS pass transistor switch ? 5
(d) What are the different colour mask used for fabrication of CMOS inverter with N-well process ? 5

2. (a) Draw the circuit diagram, stick diagram and layout using λ-based design rules for two inputs CMOS NAND gate. Use proper aspect ratio and colour coding. 10
(b) PMOS transistor was fabricated on n-type substrate with bulk doping density of $N_D = 10^{16}/cm^3$, gate doping density (n-type poly) of $N_D = 10^{20}/cm^3$, $\frac{Q_{ox}}{q} = 4 \times 10^{10}/cm^2$ and oxide thickness of tox = 0·1 μm. Calculate the threshold voltage at room temperature for $V_{SB} = 0$. 10

3. (a) Explain the method to design 8:1 multiplexer using transmission gate. Draw complete diagram using transmission gate. 10
(b) Draw stick diagram for the circuit designed to in part 3(a). 10

4. (a) Compare two scaling methods – (i) constant field and (ii) constant voltage scaling. On particular show analytically how drain current, power dissipation and power density is affected in terms of scaling. 10
(b) What is the need of burried and butting contacts ? Which technology they are needed ? Explain and compare them, used proper examples. 10

5. (a) What do you mean by threshold voltage of MOSFET ? How do we control ? Explain with the help of relevant mathematical equations. 10
(b) Compare Resistive load, Depletion load and Enhancement load NMOS inverters. 10

6. (a) Give the main features of Xilinx XC9500 CPLD family. 10
(b) Explain the latch-up in CMOS. What are the remedies to avoid the latch-up ? 10

7. (a) Design the circuit described by the function $y = \overline{A \cdot (B+C)\ (D+E)}$ using CMOS and NMOS logic. Also draw the stick diagram. 10
(b) Write the VHDL code for 4-bit full adder. 10

****